al. (U.S. Pat. No. 6,020,229).

This rejection is respectfully traversed in view of the following discussion.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

Attached hereto is a marked-up version of the changes made to the specification and/or claims by the current Amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**."

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by claim 1, is directed to a semiconductor device.

The semiconductor device includes a plurality of transistors having different gate insulator film in their thickness value, the plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The plurality of types of transistors comprises a first lightly doped drain region. The gate electrode includes an impurity to suppress depletion when forming a source region and a drain region, and one of the source region and the drain region is thinner than the other region. (See Page 5, lines 1-10; Page 10, line 19-Page 11, line 7; Page 12, line 20-24; Page 13, lines 1-7; and Figure 3(I)-(L)).

Conventional NMOSFET devices include the same gate electrode as a mask for both the core-purpose MOSFET and the I/O-purpose MOSFET. However, these devices restrict energy (ion) implantation into the lightly doped drain region making it very problematic to dope an impurity to a deep level thus forming shallow lightly doped drain regions with strong electric fields at the drains, which increase breakdown effects and give rise to hot carriers deteriorating the reliability of the device. (See Page 3, lines 3-8; Page 8, line 20-Page 9, line 5; Page 12, lines 1-10).

An aspect of the inventive structure is a first lightly doped drain region and a gate electrode includes an impurity to suppress depletion when forming a source region and a drain region, and one of the source region and the drain region is thinner than the other region, which reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. (See Page 5, line 1-10; Page 12, lines 20-25; and Page 13, lines 1-7).

As a result of this invention, the resultant structure provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance. (See Page 5, lines 7-10; Page 12, lines 11-25).

II. THE PRIOR ART REJECTIONS

A. The 102(e) Rejection Based on Yamane

As noted above, in Applicant's invention (e.g., as defined by Claim 1), the transistors include lightly doped drain regions. In particular, one of the transistors, e.g., an I/O-purpose MOSFET, for example, as cited in claim 9, includes a first lightly doped drain region. Similarly, a second transistor, e.g., a core-purpose MOSFET, for example, as cited in claim

10, includes a second lightly doped drain region. The first lightly doped drain region is deeper than the second lightly doped drain region, for example, as cited in claim 8, as the I/O-purpose MOSFET has a thicker gate electrode, which is used to form the first lightly doped drain region, compared to the core-purpose MOSFET's thin gate electrode and resultant shallower second lightly doped drain region. (See Page 12, lines 20-25; and Figures 3(I)-(L)). In addition, a gate electrode includes an impurity to suppress depletion when forming a source region and a drain region, and one of the source region and the drain region is thinner than the other region, i.e., the core-purpose MOSFET has a thinner gate. (See Page 13, lines 1-7).

In contrast, as shown in Figure 10 of Yamane, et al. ("Yamane"), Yamane merely discloses a semiconductor device, and manufacturing method, including a contact area between a thin film conductive film and a metal wiring layer for use in a non-volatile semiconductor memory. In particular, the semiconductor device includes a peripheral transistor and a LV transistor. (See Yamane at Abstract; and Column 1, lines 5-11). Each transistor includes a polysilicon film and a gate insulator film as well as a diffusion layer. As depicted in Figures 8B and 8C, the "diffusion layers 213 of the source and drain regions are formed with desired impurity concentration."(See Column 6, lines 57-67; and Column 9, lines 40-50; and Figures 8B and 8C). However, Yamane does not disclose that one of the source region and the drain region is thinner than the other region, i.e., the core-purpose MOSFET has a thinner gate as taught in Applicant's invention. Accordingly, Yamane discloses or suggests a conventional structure with a conventional diffusion layer shape where the diffusion layers appear to be the same depth as the diffusion layers may likely be formed at the same time from the same mask. (See Figures 8-10).

However, this conventional structure is unsuitable for achieving at least two objects of the invention, which are to suppress, efficiently, the occurrence of a hot carrier and optimize high-voltage reliability. (See Page 5, line 1-10; and Page 12, lines 20-25). Since this conventional structure discloses the formation of diffusion layers not lightly doped drain regions as with Applicant's invention, to one of ordinary skill in the art, these conventional diffusion layers have different characteristics than the lightly doped drain regions. In particular, Yamane's diffusion layers are substantially the same depth and appear, to one of ordinary skill in the art, to disclose a physical geometry of a conventional n+ drain contact due to being formed about the same time from the same mask independent of the thickness of the gate electrode. Yamane does not explicitly disclose or suggest separate formation of the diffusion layers. In contrast, as indicated above, Applicant's lightly doped drain regions have different depths due to being separately formed specifically based on the thickness of the individual transistor's gate electrode. (See Semiconductor Physics and Devices Basic Principles, Donald A. Neamen, IRWIN, 1992, Pages 588-590 and Figures 13-25 through 13-26; Yamane, Column 9, lines 35-50 and Figures 8A and 8B; and Application, Page 10, line 19-Page 11, line 7, and Page 12, lines 11-19). Applicant also teaches a gate electrode which includes an impurity to suppress depletion when forming a source region and a drain region, and one of the source region and the drain region is thinner than the other region, i.e., the core-purpose MOSFET has a thinner gate. (See Page 13, lines 1-7).

Similar to conventional structures (as indicated above) with shallow lightly doped drain regions, Yamane's structural arrangement may likely cause strong electric fields at the drains giving rise to hot carriers deteriorating the reliability of the device especially due to the presence of diffusion layers of the same depth. (See Page 3, lines 3-8; Page 8, line 20-Page 9,

line 5; Page 12, lines 1-10). Accordingly, Yamane teaches that the thin film polysilicon film includes a small parasitic capacitance to attain high-speed operation and high reliability for use as a resistance element. (See Yamane at Abstract; Column 2, line 65-Column 3, line 15; Column 6, lines 40-48).

Applicant's invention, however, is not shown by Yamane. Instead, Applicant teaches transistors include a first lightly doped drain region and a gate electrode which includes an impurity to suppress depletion when forming a source region and a drain region, and one of the source region and the drain region is thinner than the other region. This first lightly doped drain region is deeper compared to a second lightly doped drain region of another transistor, e.g., a core-purpose MOSFET. (See Page 12, lines 20-25; Page 13, lines 1-7; and Figures 3(I)-(L)). Accordingly, Applicant's invention efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability and increases the process margin of the gate etching during manufacturing to improve performance. (See Page 5, line 1-10; and Page 12, lines 11-25).

For at least the reasons outlined above, Applicant respectfully submits that Yamane does not teach or suggest all the features of claim 1. Accordingly, Yamane does not anticipate or render obvious the subject matter of claim 1. Withdrawal of the rejection of claim 1 under 35 U.S.C. § 102(e) as anticipated by Yamane is respectfully requested.

Finally, regarding the dependent claims, 2- 3, which depend from claim 1, these claims are patentable not only by virtue of their dependency from their respective independent claim but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited reference.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-3 and 7-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 12/13/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

1. (Amended) A semiconductor device comprising:

a plurality of [types of] transistors [having] comprising different gate insulator film in their thickness value, said plurality of [types of] transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof[;],

wherein said plurality of transistors comprise a first lightly doped drain region, and

wherein said gate electrode includes an impurity to suppress depletion when forming a source region and a drain region, and one of said source region and said drain region is thinner than the other region.

2. (Amended) The semiconductor device according to claim 1, wherein said plurality of [types of] transistors [consists of] comprise a plurality of [types of] MOSFETs formed on a substrate.

3. (Amended) The semiconductor according to claim 2,

wherein[:] said MOSFET [including] includes a core-purpose MOSFET and an I/O-purpose MOSFET[;], and

wherein said core-purpose MOSFET has a smaller thickness of [the] said gate insulator film than that of said I/O-purpose MOSFET and [the] also has a smaller thickness of [the] said gate electrode than that of said I/O-purpose MOSFET.